



Welcome United States Patent and Trademark Office

☐ Search Results[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Results for "(((hardware) &lt;near/12&gt; (multithread\*, thread\*) &lt;and&gt; stack\*)&lt;in&gt;metadata)"

☒ e-mail

Your search matched 6 of 1489021 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

## » Search Options

[View Session History](#)[New Search](#)

## Modify Search

(((hardware) &lt;near/12&gt; (multithread\*, thread\*) &lt;and&gt; stack\*)&lt;in&gt;metadata)

[Search](#) >☐ Check to search only within this results set

Display Format:

☒ Citation☐ Citation & Abstract

## » Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

[view selected items](#)[Select All](#) [Deselect All](#)

- ☐ 1. **An Interprocedural Code Optimization Technique for Network Processors Using Hardware N Support**  
Scharwaechter, H.; Hohenauer, M.; Leupers, R.; Ascheid, G.; Meyr, H.;  
[Design, Automation and Test in Europe, 2006. DATE '06. Proceedings](#)  
Volume 1, 6-10 March 2006 Page(s):1 - 6  
[AbstractPlus](#) | Full Text: [PDF\(144 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ 2. **Context threading: a flexible and efficient dispatch technique for virtual machine interpreter**  
Berndl, M.; Vitale, B.; Zaleski, M.; Brown, A.D.;  
[Code Generation and Optimization, 2005. CGO 2005. International Symposium on](#)  
20-23 March 2005 Page(s):15 - 26  
Digital Object Identifier 10.1109/CGO.2005.14  
[AbstractPlus](#) | Full Text: [PDF\(240 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ 3. **Fair cache sharing and partitioning in a chip multiprocessor architecture**  
Kim, S.; Chandra, D.; Solihin, Y.;  
[Parallel Architecture and Compilation Techniques, 2004. PACT 2004. Proceedings. 13th Internation](#)  
29 Sept.-3 Oct. 2004 Page(s):111 - 122  
Digital Object Identifier 10.1109/PACT.2004.1342546  
[AbstractPlus](#) | Full Text: [PDF\(442 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ 4. **Hardware support for control transfers in code caches**  
Kim, H.-S.; Smith, J.E.;  
[Microarchitecture, 2003. MICRO-36. Proceedings. 36th Annual IEEE/ACM International Symposiur](#)  
2003 Page(s):253 - 264  
Digital Object Identifier 10.1109/MICRO.2003.1253200  
[AbstractPlus](#) | Full Text: [PDF\(440 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ 5. **A dynamic multithreading processor**  
Akkary, H.; Driscoll, M.A.;  
[Microarchitecture, 1998. MICRO-31. Proceedings. 31st Annual ACM/IEEE International Symposiur](#)  
30 Nov.-2 Dec. 1998 Page(s):226 - 236  
Digital Object Identifier 10.1109/MICRO.1998.742784

[AbstractPlus](#) | [Full Text: PDF\(108 KB\)](#) [IEEE CNF](#)  
[Rights and Permissions](#)



6. **A dualthreaded Java processor for Java multithreading**

Chun-Mok Chung; Shin-Dug Kim;

Parallel and Distributed Systems, 1998, Proceedings., 1998 International Conference on

14-16 Dec. 1998 Page(s):693 - 700

Digital Object Identifier 10.1109/ICPADS.1998.741157

[AbstractPlus](#) | [Full Text: PDF\(140 KB\)](#) [IEEE CNF](#)  
[Rights and Permissions](#)

[Help](#) [Contact Us](#) [Privac](#)

© Copyright 2006 IE

Indexed by  
 Inspec